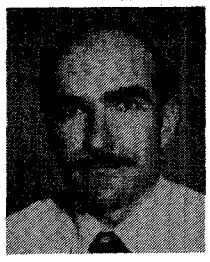

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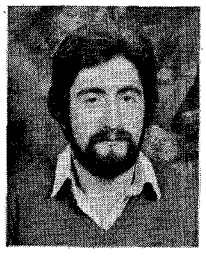

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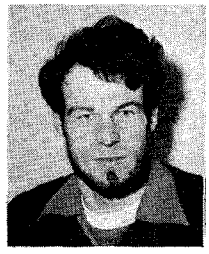

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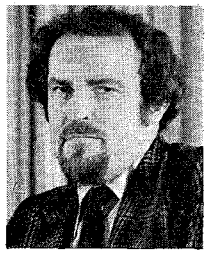

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A New Approach to the Computer-Aided Design of Nonlinear Networks and its Application to Microwave Parametric Frequency Dividers

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***Abstract*—A new cost-effective method allowing nonlinear microwave circuits to be designed by computer is demonstrated by application to parametric frequency dividers. The method is based on frequency-domain representations of both nonlinear circuit components and network voltages and currents. A special optimization strategy determines the unknown parameters of the linear part of the circuit while eliminating the need for a complete analysis of the nonlinear network at each step of the iterative process.**

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I. INTRODUCTION

IN THIS PAPER we demonstrate a new, very effective approach to the computer-aided design of nonlinear networks by working out in detail a specific microwave design problem and showing the experimental validity of the solutions obtained. The circuit to be dealt with—the

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parametric frequency divider—can be considered as typically representative of a broad class of nonlinear microwave subsystems from our present standpoint, since its considerable technical interest is in contrast with a substantial lack of systematic design information from the literature. In fact, a hybrid integrated frequency divider commonly represents the first stage of the dividing chain used to stabilize an RF oscillator by phase-locking to a low-frequency reference source, and this will be the case at high microwave frequencies until the development of GaAs technology will make monolithic digital dividers commercially available. In particular, parametric dividers using microwave diodes often represent an optimum choice because of their broader bandwidth and simpler circuit configuration, in comparison with other types, such as the Miller or the injection-locked ones. On the other hand, classic treatments [1], [2] only give a general feeling of the principles of device operation, while more recent works [3]–[5] seem to be mostly aimed at the discussion of empirical results, and do not attempt to overcome traditional simplified analyses. Thus, they are of limited help to the microwave engineer faced with a practical divider design problem.

On the contrary, this paper outlines a straightforward approach leading to accurate and reliable designs ready for MIC realization through the use of modern nonlinear computer-aided analysis techniques. A few distinctive features of the new method are worth mentioning. First, we employ a circuit model of the nonlinear device accounting for all essential aspects of its large-signal behavior as well as for parasitic effects. For the parametric divider, this makes it possible to cope with such cases as the use of varactors strongly driven into forward conduction or even step-recovery diodes, which often occur in modern applications. Furthermore, all voltages and currents are represented as superpositions of several harmonic components, all of which are simultaneously taken into account in the analysis and optimization. In most cases this is strictly necessary for the results of the computer analysis to be physically significant; as an example, at least six harmonics of the output frequency are needed to study a parametric divider by two with zero- or forward- biased diodes. Finally, a new optimization philosophy has been devised in order to solve the problem of designing by computer a nonlinear circuit with reasonable effort in terms of CPU time. The basic concept is to eliminate the need for a complete analysis of the nonlinear network at each step of the iterative search for the unknown circuit parameters.

Generally speaking, the technique described in this paper is believed to represent one of the most powerful tools that are presently available for nonlinear network design, and is well suited for application to broad classes of active microwave circuits.

II. Diode Model

An accurate simulation of the microwave diode clearly represents one of the key conditions for the validity of the computer-aided approach. Fig. 1 shows an adequate circuit model, including parasitic effects, the diode series resistance, and the p-n junction as separate circuit elements. Package parasitics are usually available from the data sheets and may be regarded as known. As for the series resistance, strictly speaking it should be treated as a voltage-dependent nonlinear element [6]. However, in typical applications its absolute change corresponding to the actual voltage swing across the junction is small, so that taking it as a constant does not lead to appreciable errors. To illustrate this point we consider a specific abrupt-junction Silicon epitaxial varactor (ALPHA DVA 6733-07), and report in Table I some data provided by the manufacturer. When using this diode in the parametric divider described in Section V at an input power level of 9 dBm, the junction voltage ranges approximately from -1.5 V to 0.6 V, so that change of R_s is less than 0.1 Ω. Thus, we are left with only one nonlinear component, the p-n junction, which can be described by the equation

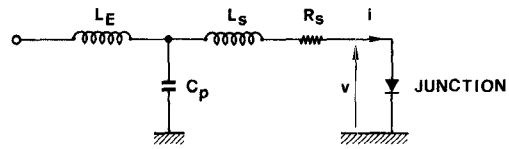

Fig. 1. Circuit model of a packaged varactor diode.

TABLE I

ALPHA DVA 6733-07	
v ≥ 0.8 V	$R_S \simeq 0.64\ \Omega$
v = −4 V	$R_S \simeq 0.51\ \Omega$

$$i = I_s\left[\exp\left(\frac{ev}{nK_BT}\right)-1\right]+\frac{d}{dt}[q(v)] \tag{1}$$

where

- i diode current;
- v voltage across the junction;
- q total stored charge;
- I_s saturation current;
- e electron charge;
- n slope factor (or "ideality factor") of current;
- K_B Boltzmann's constant;
- T absolute temperature.

In general, there will be two main contributions to the stored charge, that is, the depletion-layer charge q_T and that due to the injected minority carriers q_D so that

$$q(v) = q_T(v) + q_D(v). \tag{2}$$

Concerning the former, we first note that the depletion-layer differential capacitance is usually a known function of the applied voltage for a given diode. For idealized doping profiles such as the step or the linear junction, this function takes the well known analytic form

$$\frac{dq_T}{dv} = C_{T0}\left(1-\frac{v}{\phi}\right)^{-\gamma} \tag{3}$$

$(0<\gamma<1)$, where ϕ is the diffusion potential, and C_{T0} is the zero-bias transition capacitance. Thus, in such cases we find

$$q_T(v)=C_{T0}\frac{\phi^{\gamma}}{\gamma-1}(\phi-v)^{1-\gamma}. \tag{4}$$

Both (3) and (4) are only valid for $v<\phi$, taking forward voltages as positive. Note that (4) yields $q_T\to 0$ for v approaching ϕ, because of the assumption $\gamma<1$. This is consistent with the physical picture of diode operation, since at $v\geqslant\phi$ the depletion layer vanishes. To complete the definition of the depletion-layer charge we thus associate (4) with the equation

$$q_T(v)=0, \qquad v\geqslant\phi. \tag{5}$$

For realistic doping profiles obtained from practical technological processes, a simple closed-form expression such as (3) is no longer usable unless γ itself be considered as a function of the applied voltage. This includes hyper-abrupt-junction diodes [6], which can be represented by (3) with $\gamma>1$ only in a limited range of reverse-bias voltages. In similar cases, (3) is replaced by an empirical relationship which is usually supplied by the manufacturer, most often in graphic form. The latter can be approximated by a polynomial expression, so that the explicit dependence of the depletion-layer charge on the applied voltage may once again be obtained by integration. As for the injected carrier capacitance, we revert to classic analyses of charge-storage diodes, such as Moll's [7], to find the following expression which is simple and accurate enough for our present purposes:

$$q_D(v)=I_s\tau\exp\left(\frac{ev}{nK_BT}\right). \tag{6}$$

In (4), τ represents the average minority-carrier lifetime and is given by the manufacturer. The current arising from (6) represents an important contribution to the total current for a junction diode operated under zero- or forward-bias conditions. In these cases, the strong nonlinearity of (6) usually turns out in a significant improvement of power-handling ability , and possibly of circuit efficiency. Furthermore, through (1) and (6) the simulation of step-recovery diodes becomes possible [8]. In such devices, the storage capacitance dominates [7], that is, on the average q_D is large in comparison with q_T, and the depletion-layer capacitance merely acts as a parasitic effect.

A final point concerns a purely numerical aspect of our model which is noteworthy in view of its practical implementation on a computer. In both (6) and (1) there appears the exponential function

$$F(v)=\exp\left(\frac{ev}{nK_BT}\right) \tag{7}$$

whose argument is the ratio of the computed voltage across the junction to the thermal voltage nK_BT/e. Since the latter is of the order of 0.03 V for a junction operated at room temperature and $n\cong 4/3$ [7], numerical overflow of (7) is likely to occur in the early stages of the optimization, especially in the case of a forward-biased diode. To avoid this, we first choose a threshold voltage V_T, which has to be larger than any forward voltage that can physically exist across the junction, but still small enough so that the exponential at threshold falls well within the computer range. As an example, for a Cyber 76 computer system we can take

$$\frac{eV_T}{nK_BT}=100 \tag{8}$$

yielding $V_T\cong 3.5$ V and $F(V_T)\cong 3\times 10^{43}$. Then we replace $F(v)$ above threshold by a parabola $P(v)$ of the form

$$P(v)=F(V_T)\cdot\left[1+\left(\frac{ev}{nK_BT}-100\right)+\frac{1}{2}\left(\frac{ev}{nK_bT}-100\right)^2\right] \tag{9}$$

which ensures the continuity of the first and second derivatives at the threshold point. Any danger of overflow is thus eliminated while preserving the accuracy of the model in the range of physically significant voltages.

III. Circuit Analysis

A general schematic representation of the device to be dealt with is given in Fig. 2. The linear network includes any required passive components such as idlers, filters, couplers, and so on, as well as the diode series resistance (which is assumed to be constant) and package parasitics. For a frequency divider by m (integer) with an output frequency f_o, only one sinusoidal source (or pump generator) at a frequency

$$f_p=mf_o \tag{10}$$

will appear in the network. This generator is explicitly put into evidence in the circuit diagram together with the bias and load. Note that the same drawing is equally good for representing a frequency multiplier instead of a divider, provided that the pump and output frequencies are interchanged in (10). In much the same way, the following analytical developments are generally applicable to the design of parametric multipliers as well as dividers.

For any given passive network, a steady-state analysis of the circuit may be carried out by a suitable application of the well-known harmonic-balance technique [9]–[11]. According to this method, the current and voltage across the junction are expressed as superpositions of harmonics of the output frequency f_o with unknown complex amplitudes; that is

$$\begin{aligned} i(t)&=\mathrm{Re}\left\{\sum_{K=0}^{N} I_K\exp(jK\omega_0 t)\right\}\\ v(t)&=\mathrm{Re}\left\{\sum_{K=0}^{N} V_K\exp(jK\omega_0 t)\right\} \end{aligned} \tag{11}$$

where $\omega_0=2\pi f_o$ and N is the number of frequency components (not including dc) which are assumed to be signifi-

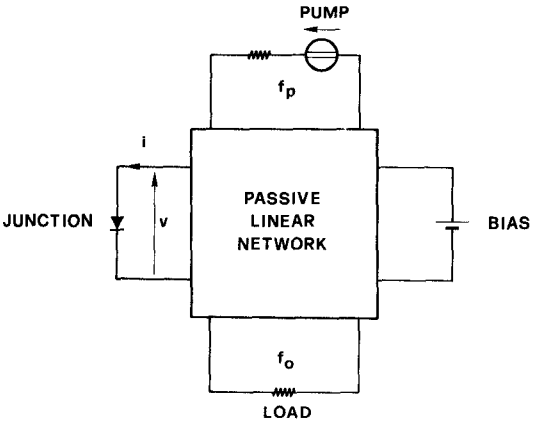

Fig. 2. Schematic representation of parametric frequency divider or multiplier.

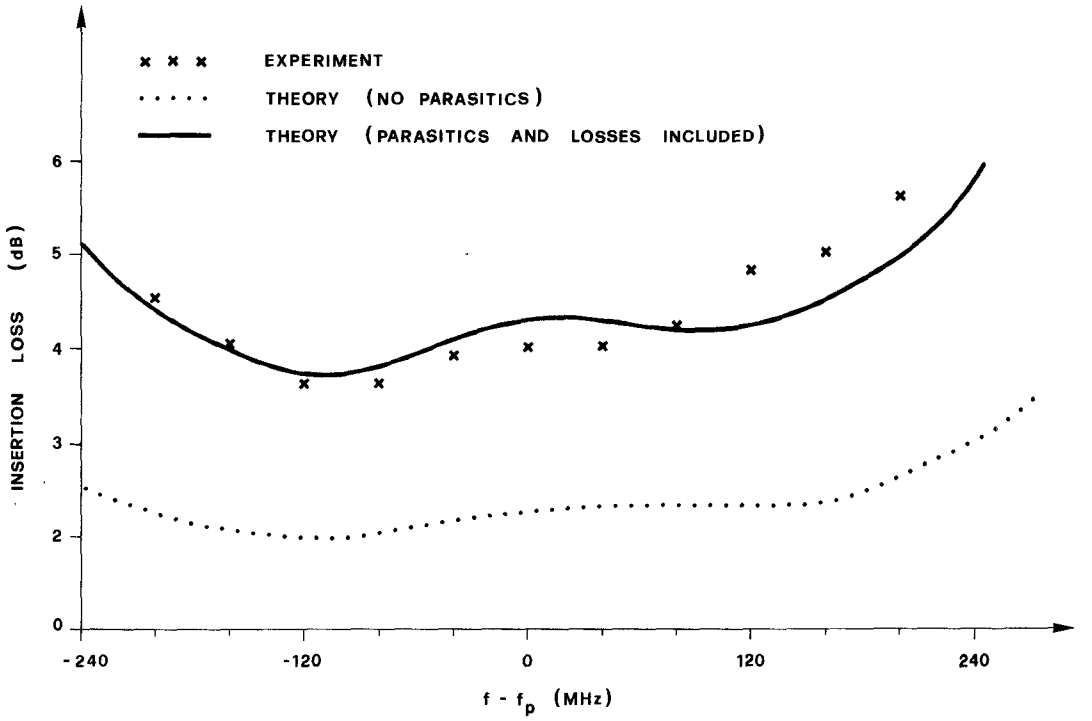

Fig. 3. Voltage waveforms across the diode junction for a typical microstrip divider by 2. N represents the number of harmonic frequency components that are considered significant.

cant. If we let

$$J(v)=I_s\left[\exp\left(\frac{ev}{nK_BT}\right)-1\right] \tag{12}$$

the diode equation (1) may be rewritten in the form

$$i=J(v)+\frac{d}{dt}[q(v)] \tag{13}$$

where the conduction and displacement components of the current are put into evidence. If we now select a vector of voltage harmonics

$$V\equiv[V_K] \tag{14}$$

then, through (11), $J[v(t)]$ and $q[v(t)]$ are automatically known in the time domain, and are obviously periodic with the same period $1/f_o$ as the applied voltage. Thus, we make use of a Fourier expansion and still retain only N frequency components to obtain

$$J[v(t)]=\mathrm{Re}\left\{\sum_{K=0}^{N} J_K\exp(jK\omega_0 t)\right\}$$

$$q[v(t)]=\mathrm{Re}\left\{\sum_{K=0}^{N} Q_K\exp(jK\omega_0 t)\right\} \tag{15}$$

where J_K and Q_K are actually computed by means of the Fast-Fourier-Transform algorithm. From (13) the current harmonics are expressed as

$$I_K=J_K+jK\omega_0 Q_K=G_K(V), \qquad K=0,1,\cdots,N \tag{16}$$

where G_K is a (numerically) known nonlinear function of V. The set of equations in (16) can be considered as the frequency-domain description of the nonlinear device, playing the same role as the basic equation (1) does in the time domain. (16) can be combined with the equations of the linear part of the network

$$V_K = -Z(jK\omega_0)I_K + U_K, \qquad K = 0,1,\cdots,N \quad (17)$$

to obtain a nonlinear solving system of $2N+1$ real equations in as many unknowns of the form

$$\{V_K + Z(jK\omega_0)G_K(V) - U_K = 0, \qquad K = 0,1,\cdots,N. \quad (18)$$

This system is always nonhomogeneous since the known term U_K is nonzero for $K=0$ and $K=m$ $Z(j\omega)$ obviously represents the impedance of the linear network as seen at the diode terminals. Once a solution of (18) has been found, all quantities of interest such as the divider efficiency and return loss can be derived by a conventional analysis of the linear network.

The number of frequency components which are assumed to be significant obviously represents a key parameter since it determines the tradeoff between accuracy and cost of the computer analysis. Usually the best compromise must be established empirically. As an example, by examining the dependence on N of the overall circuit performance, it was found that $N=6$ turns out to be a consistent choice for the divider by 2. This is illustrated in Fig. 3, showing a comparison of the voltage waveforms across the diode for a microstrip divider having a 30-percent efficiency at an input power level of 9 dBm and zero bias, in the cases $N=10$, $N=6$, and $N=2$. The $N=6$ computations clearly provide very satisfactory results, while for $N=2$ the accuracy is poor. An interesting consequence is that meaningful results can hardly be expected from classic closed-form analyses based on the two-frequency approximation [1]–[2], at least in the case of zero- or forward-biased diodes.

IV. Circuit Design

From the design point of view, we first note that most previous approaches to the computer optimization of nonlinear networks (e.g., [12]–[15]) comply with the general philosophy outlined in Fig. 4[1]. These methods may substantially differ from one another, mainly in the way they update the values of the unknowns after an unsatisfactory test, but the basic flow-chart always remains the same. This kind of approach is usually far too expensive to be practically feasible, and it is not very difficult to understand why this is the case. In fact, the nonlinear design problem faces us with two distinct sets of unknowns and related specifications; that is, the voltage harmonics, which must be selected in such a way as to obtain the harmonic balance according to (18), and the circuit parameters, to be determined so that the design specifications are met. In any conventional optimization approach, the first set of unknowns is granted a higher priority mainly for physical reasons, in order to preserve the physical meaning of the network functions during the optimization. Clearly, this happens only if the harmonic balance is found (i.e., the system (18) is solved) prior to each function evaluation. Since solving (18) is substantially equivalent to carrying out an optimization with respect to the V_K's, the result is two nested optimization loops, the inner one providing the objective function for the outer, which is clearly not a healthy way of solving a computer-aided design problem.

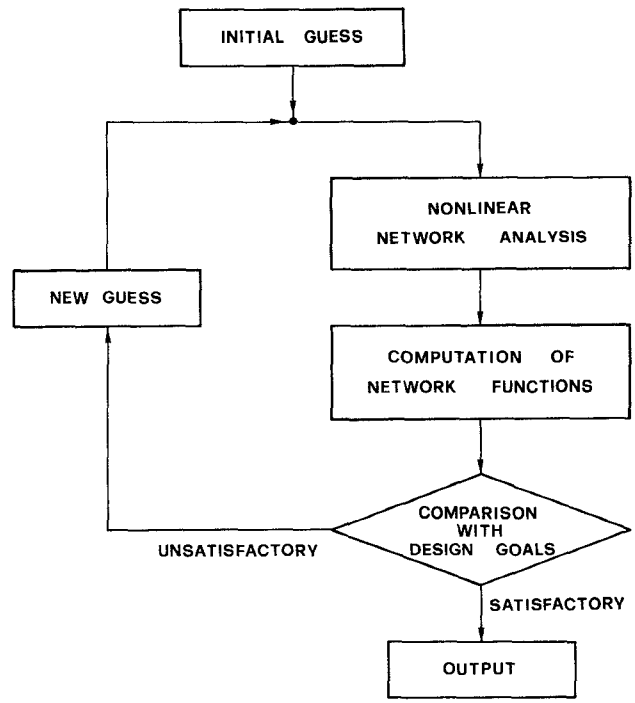

Fig. 4. General flow-chart of conventional algorithms for nonlinear network design.

As an efficient alternative, we assume that all unknowns are equivalent, and carry out a simultaneous search for both the voltage harmonics and the electrical parameters of the linear network by minimizing an objective function defined as a combination of the electric performance specifications and of the harmonic-balance requirement. In this way, the network functions during the optimization are only mathematically significant, because they are not associated with any electrical regime that the network can support, but get back their original physical meaning once the optimization has been successfully completed, since then the harmonic balance is reestablished.

To illustrate this technique, we now discuss the analytic formulation of the problem in the case of a parametric divider to be designed for a minimum prescribed efficiency and return loss. Let the vector of unknown circuit parameters be represented by $\boldsymbol{P}$, and the divider efficiency and return loss by η and L_R, respectively. Thus, the total set of unknowns may be indicated as $(\boldsymbol{V},\boldsymbol{P})$, where $\boldsymbol{V}$ is defined by (14). For any given passive network (i. e., for any vector

[1]We denote by "network function" any quantity used to describe circuit performance such as efficiency, return loss, and so on.

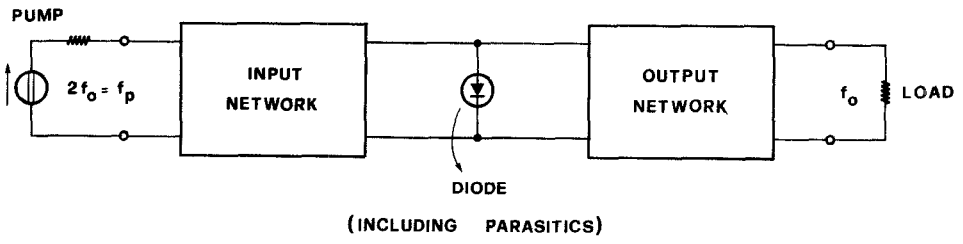

Fig. 5. Schematic topology of microstrip parametric divider.

$\boldsymbol{P}$), both the impedance $Z(j\omega)$ and the Thévenin voltages U_K appearing in (17), (18) can be found directly. If we further select a vector $\boldsymbol{V}$ of voltage harmonics, the associated electrical regime of the passive network can be analyzed to obtain the efficiency and return loss. In this sense, η and L_R can be treated as known functions of ($\boldsymbol{V}$, $\boldsymbol{P}$). At this stage the objective function to be minimized can be expressed as

$$F_{OB}(\boldsymbol{V},\boldsymbol{P}) = A(\eta,\eta_{\mathrm{MIN}},W_\eta) + A(L_R,L_{\mathrm{MIN}},W_L) + \left\{\sum_{K=0}^{N} |V_K + Z(jK\omega_0,\boldsymbol{P})G_K(\boldsymbol{V}) - U_K(\boldsymbol{P})|^2\right\}^{1/2} \tag{19}$$

where η_{MIN}, L_{MIN} are the minimum acceptable efficiency and return loss, and

$$A(x,x_{\mathrm{MIN}},W) = \begin{cases} [W(x-x_{\mathrm{MIN}})]^4, & x < x_{\mathrm{MIN}} \\ 0, & x \geq x_{\mathrm{MIN}} \end{cases}. \tag{20}$$

In (19) and (20), the quantities W_η, W_L, and W represent suitable weighting factors. For a broadband design, we simply add to the objective function a contribution of the form (19) for each one of a number of discrete frequencies selected within the band of operation. Failure to attain a minimum of the objective function close enough to zero indicates that the design goals cannot be met. Most likely this denotes an improper combination of pump available power, minimum efficiency or return loss, and diode choice for the frequency range of interest; a typical such case occurs, for instance, when the input power is lower than the operating threshold. Note that in some cases the diode bias voltage can be used as a design variable, providing a further degree of freedom and a better conditioning of the optimization problem.

The present formulation of the nonlinear design problem has several advantages with respect to the conventional approach described in Fig. 4. First of all, the design cost is dramatically reduced. Though it is not easy to give a general evaluation of the amount of computer time that can be saved by the above technique, in principle one can expect to obtain a complete design at much the same cost as one function evaluation of the conventional method. In the parametric divider case, a reliable estimate is that the CPU time can be reduced by about two orders of magnitude, thus turning an exceedingly expensive design into a cost-effective one. A related point is that specially tailored optimization algorithms are usually not necessary, since the problem is well within the reach of standard "off-the-shelf" minimization routines. This can speed up considerably the implementation of a practical design, and thus be of much help to the microwave engineer.

Finally, extensive computations showed that the new algorithm exhibits an excellent stability from the numerical point of view. Whenever a physically defined solution exists, it is truly unique, and can be arrived at from any arbitrarily selected starting point. This is of special importance for such applications as parametric divider design, for which no significant starting-point information is usually available. In particular, this allowed an initial value of zero to be systematically used for the voltage harmonics in most divider calculations.

V. A Design Example

As an example of application, we describe a practical microstrip divider by two which was designed by the method outlined in the preceding sections. This divider was devised to act as the first step of the PLL used to lock the tunable RF source of an FM radio link [16] to a 4-MHz reference oscillator. The design goals were: a bandwidth of about 20 percent with an input center-band frequency $f_p = 2f_o = 2.375$ GHz[2]; an insertion loss in the 4- to 6-dB range (in a 50-Ω environment) and a return loss in the 10-dB range at an input power level of 9 dBm; a minimum isolation of 15 dB between the input and output ports throughout the operating band.

As a first step we chose the circuit topology schematically illustrated in Fig. 5. The input network should act as a matching network of bandpass type, also providing isolation between the pump and the signals generated by the diode at frequencies different from f_p. Since no significant starting-point information was available, this network was initially designed as a conventional commensurate-line bandpass filter with short-circuited stubs $\lambda/4$ long at f_p, having an attenuation larger than 20 dB across the output band ($f_o \pm 10$ percent) and an impedance level of 50 Ω. Similarly, the output network was designed as a low-pass filter of the stepped-impedance type with a cutoff frequency $1.1\,f_o$ and an attenuation larger than 20 dB across the input band ($f_p \pm 10$ percent). Finally, an abrupt-junction Silicon

[2]At the time when these dividers were designed and manufactured (January 1981), the fastest digital divider available on the market was a 1.6-GHz device from Plessey.

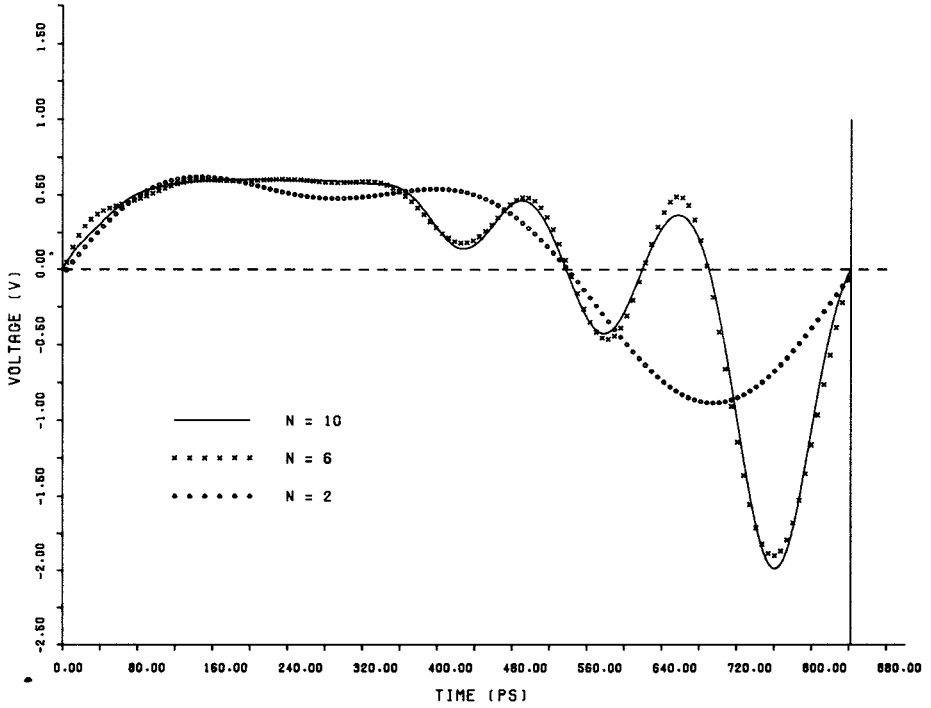

Fig. 6. Computed and measured insertion loss of microstrip parametric divider ($P_{in} = 9$ dBm).

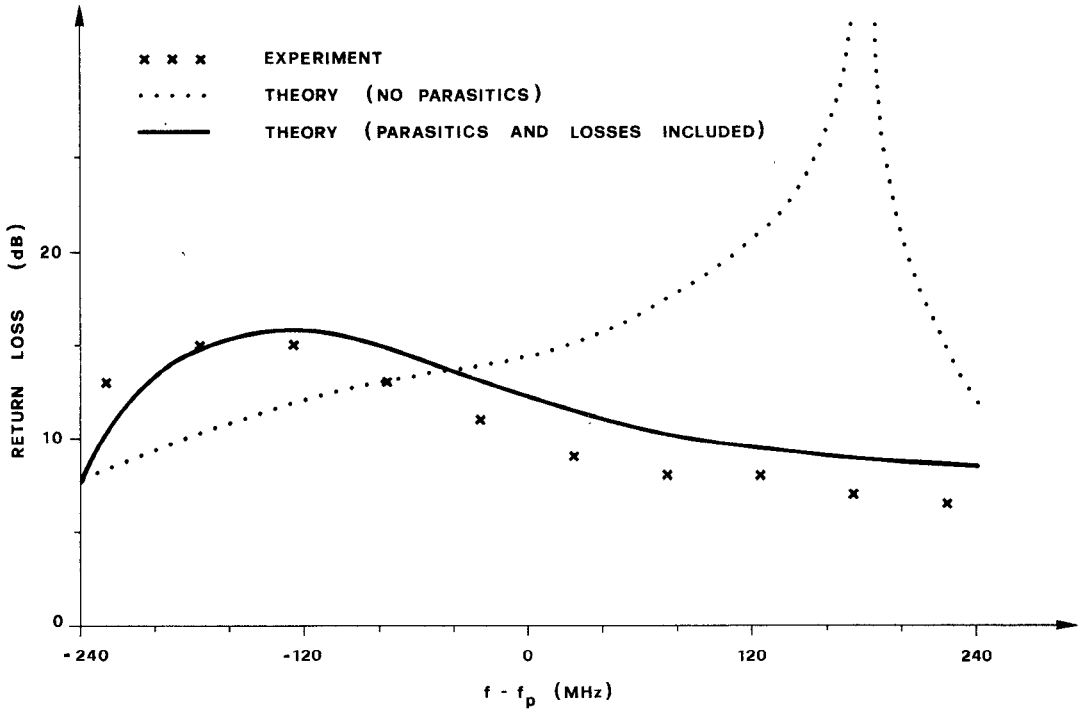

Fig. 7. Computed and measured return loss of microstrip parametric divider ($P_{in} = 9$ dBm).

epitaxial varactor (ALPHA DVA 6733-07) with a quality factor of about 90 at f_p and a zero-bias depletion-layer capacitance $C_{T0} = 3.3$ pF was selected both for the sake of availability and because of its favourable impedance level at f_p.

An analysis of this preliminary circuit arrangement by means of (18) showed that no frequency division would take place in this network, since the only possible solution had $V_1 = 0$. As could be expected, selecting at random and assembling two filters and a diode does not mean building a frequency divider; in fact a low-efficiency frequency multiplier is generally obtained instead. Then the design procedure described in Section IV was applied using this circuit as a starting point. In order to save CPU time, only

three frequencies (i.e., the upper and lower bounds and the center of the band of operation) were considered in the optimization. Furthermore, preliminary design steps were carried out with a small fixed number of iterations and a very limited number of variable circuit parameters (usually one in the input and one in the output network) in order to find out the most critical ones. In the final run, eight circuit variables and six frequency components (see Fig. 3) were optimized by a standard conjugate–gradient algorithm. The diode bias voltage was arbitrarily kept to zero (i.e., $U_0 = 0$ in (19)) in order to eliminate any sort of bias network in the circuit.

The resulting network, which was built on DUROID substrate by microstrip techniques, provided frequency division across the prescribed band with a maximum insertion loss of about 5.5 dB and an operating threshold in the 3-mW range. The computed performance of this divider is displayed in Figs. 6 and 7, where a comparison with experimental results is also provided. The dotted lines in these figures were obtained by neglecting losses and discontinuity effects in the microstrip network. The agreement with the measured performance of the divider is reasonable, but should be improved in at least two respects: first, the predicted insertion loss is, on the average, 2 dB lower than the measured one; second, the computed peak of the return loss hardly appears in the experimental response. It has been found that the above discrepancies may be ascribed to poor modeling of the passive network (especially at the higher harmonics, which play a nonnegligible role as discussed in Section III). In order to improve our description, the following steps were undertaken:

1) The equivalent circuits of the microstrip discontinuities were included in the calculations using the mode-matching method for the tee-junctions [17] and experimental data for the impedance steps [18].

2) Microstrip losses were accounted for making use of classic closed-form expressions [19] and of an "equivalent" conductivity of the strip conductors. The latter was determined in such a way that the measured attenuation constant of the 50-Ω line was accurately predicted by the above mentioned formulae up to about 10 GHz (thus covering up to the 6th harmonic of the output band). The results obtained in this way are plotted in Figs. 6 and 7 by solid lines; the agreement with the experimental data is now clearly excellent.

Finally, this design turned out to be very repeatable; in fact, more than 200 such dividers were built (for production purposes) and separately tested, and all of them were found to work according to the design specifications with virtually no need for tuning. The measured performance described above was actually obtained by averaging the behavior of an initial set of 50 dividers.

VI. Conclusion

The computer-aided design of linear microwave circuits can be considered a well-settled matter, as is shown by the commercial availability of powerful user-oriented CAD programs [20]. On the other hand, the general problem of nonlinear circuit design still represents a challenge for the microwave engineer, and this is probably so, at least in part, because a reasonably efficient design scheme had not been proposed so far.

In the authors' opinion the approach outlined in this paper might well represent the seed of a general-purpose program library capable of designing several types of nonlinear subsystem in a straightforward way. The basic concepts are the use of nonlinear circuit models for the semiconductor devices, the harmonic-balance analysis technique, and the simultaneous optimization of both the harmonic amplitudes and the linear circuit parameters. The discussion of these topics has been oriented here towards the solution of a specific problem, the design of parametric dividers, rather than being treated in general. This approach has been chosen in order to show that such programs already exist (though they are not yet user-oriented enough to be commercially interesting) and can be used for practical applications of technical importance. In some cases (such as parametric dividers with zero- or forward-biased diodes) the only alternative to the computer-aided approach described here is probably represented by previous experience and intuition supported by trial-and-errors techniques, which is obviously much less rewarding from the engineering point of view.

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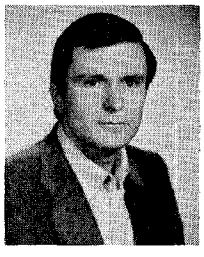

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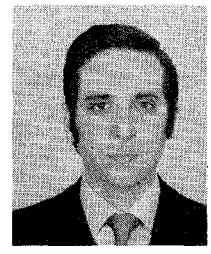

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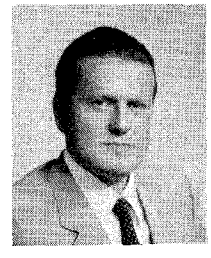

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